What is claimed is:

1. A semiconductor device comprising:

a first terminal;

a second terminal;

a power supply voltage dropping circuit that generates a constant voltage;

a switch circuit that periodically applies the constant voltage to the first terminal in response to a first clock;

an output buffer that periodically applies a power supply voltage to the second terminal in response to the first clock;

a phase adjuster circuit;

a current-controlled oscillator circuit; and

a counter,

wherein the power supply voltage dropping circuit supplies a first current to the switch circuit,

wherein the current-controlled oscillator circuit generates a second clock whose frequency changes in response to the value of the first current,

wherein the phase adjuster circuit sets a phase where the switch circuit applies the constant voltage to the first terminal, and a phase where the output buffer applies the power supply voltage to the second terminal to an in-phase period for the same phase or a reversed phase period for a reversed phase, and

wherein the counter counts the number of the second clocks in each of the in-phase period and the reversed phase period over a counting time set to the same value.

2. The semiconductor device according to claim **1**, further comprising:

a second transistor;

wherein the power supply voltage dropping circuit includes a first transistor that outputs the first current,

wherein a current mirror circuit contains the first transistor and the second transistor;

wherein the second transistor supplies a second current to the current-controlled oscillator circuit, and

wherein the frequency of the second clock changes in response to the value of the second current.

3. The semiconductor device according to claim **1**,

wherein the switch circuit is an inverter circuit.

4. The semiconductor device according to claim **3**,

wherein the value of the first current changes in response to the change in the parasitic capacitance value of the first touch electrode coupled to the first terminal and the change in the parasitic capacitance value of the second touch electrode coupled to the second terminal.

5. The semiconductor device according to claim **4**,

wherein the value of the first current changes in response to the change in the parasitic capacitance value between the first touch electrode and the second touch electrode.

6. The semiconductor device according to claim **5**,

wherein the change in the parasitic capacitance value of the first touch electrode and the second touch electrode is detected based on the difference value in the count value of the second clock over a counting time in the in-phase period, and the count value of the second clock over a counting time in the reversed phase period.

7. A semiconductor device comprising:

a first terminal;

a second terminal;

a counter; and

a switch circuit that periodically applies a constant voltage to the first terminal in response to a first clock,

wherein a power supply voltage is periodically applied to the second terminal in response to the first clock,

wherein a first current is applied to the switch circuit,

wherein a frequency of a second clock changes in response to the value of the first current,

wherein a first phase of a voltage waveform corresponding to the constant voltage applied to the first terminal and a second phase of a voltage waveform corresponding to the power supply voltage applied to the second terminal are set to be the same phase for an in-phase period, and set to be the reversed phase for a reversed phase period, and

wherein the counter counts the number of the second clocks in each of the in-phase period and the reversed phase period.

8. The semiconductor device according to claim **7**, wherein the counter counts the number of the second clocks in each of the in-phase period and the reversed phase period over a counting time set to the same value.

9. The semiconductor device according to claim **8**, further comprising:

a power supply voltage dropping circuit that generates the constant voltage;

an output buffer that periodically applies the power supply voltage to the second terminal in response to the first clock;

a phase adjuster circuit; and

a current-controlled oscillator circuit that generates the second clock,

wherein the power supply voltage dropping circuit supplies the first current to the switch circuit, and

wherein the output buffer sets the first phase and the second phase to be the same phase for the in-phase period, and the reversed phase for the reversed phase period.

10. The semiconductor device according to claim **9**, further comprising:

a second transistor;

wherein the power supply voltage dropping circuit includes a first transistor that outputs the first current,

wherein a current mirror circuit contains the first transistor and the second transistor,

wherein the second transistor supplies a second current to the current-controlled oscillator circuit, and

wherein the frequency of the second clock changes in response to the value of the second current.

11. The semiconductor device according to claim **9**, further comprising:

a second transistor;

wherein the power supply voltage dropping circuit includes a first transistor that outputs the first current,

wherein a current mirror circuit contains the first transistor and the second transistor,

wherein the second transistor supplies a second current to the current-controlled oscillator circuit, and

wherein the frequency of the second clock changes in response to the value of the second current.

12. The semiconductor device according to claim **9**,

wherein the switch circuit is an inverter circuit.

13. The semiconductor device according to claim **12**,

wherein the value of the first current changes in response to the change in the parasitic capacitance value of the first touch electrode coupled to the first terminal and the